

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/748,557	KOO, KIE-BONG	
Examiner		Art Unit		Page 1 of 1
Tuan T. Nguyen		2824		

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,426,900 B1	07-2002	Maruyama et al.	365/194
	B	US-6,424,585 B1	07-2002	Ooishi, Tsukasa	365/226
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	US 2004/0100837 (Jung-Bae Lee) May 27, 2004, On-Die Termination circuit and method for reducing on-chip DC current, and memory system including memory device using the same
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.